WHAT IS CLAIMED IS:

1. A non-volatile semiconductor storage device comprising:

a ROM region which stores fuse data;

at least one pad to which a control signal is supplied; and

a read control circuit connected to the ROM region and the at least one pad to receive a power voltage and control reading of fuse data from the ROM region after the power voltage has reached a predetermined level during a rise so as to control timing for activating an operation of reading the fuse data, according to the control signal.

2. The device according to claim 1, wherein the read control circuit includes:

a power-on level detecting circuit which receives the power voltage and detects that the power voltage has reached a predetermined level during a rise to output a power-on reset signal;

a delay circuit which is connected to the power-on level detecting circuit and the at least one pad and which has delay time controlled according to the control signal so as to delay the power-on reset signal.

3. The device according to claim 1, wherein the control signal is a chip address signal.

4. The device according to claim 2, wherein the

delay circuit includes:

a clock signal generating circuit which receives the power-on reset signal so that operation of the generating circuit is controlled according to the power-on reset signal to output a clock signal;

a counter circuit which receives and counts the clock signal; and

a decoder circuit which receives a count output from the counter circuit so that an output from the decoder circuit is changed after the counter circuit has counted a predetermined number of clock signals, the predetermined number being controlled according to the control signal.

5. The device according to claim 2, wherein the delay circuit has at least a resistance circuit and a capacitor circuit, and the delay time is controlled by varying one or both of a resistance value of the resistance circuit and a capacitance of the capacitor circuit according to on the control signal.

6. The device according to claim 1, wherein the read control circuit includes:

a power-on level detecting circuit which receives the power voltage, has a power voltage detection level controlled according to the control signal, and detects the power voltage while the power voltage is rising to output a power-on reset signal; and

a delay circuit which receives and delays the

power-on reset signal.

7. The device according to claim 6, wherein the control signal is a chip address signal.

8. The device comprising:

a fuse circuit which stores first fuse data and reads the first fuse data when a power voltage reaches a first level during a rise;

a ROM region which stores second fuse data; and

a read control circuit connected to the ROM region to receive the first fuse data and control reading of the second fuse data from the ROM region after the power voltage has reached a second level during a rise so as to control timing for activating an operation of reading the second fuse data, according to the first fuse data.

9. The device according to claim 8, wherein the first level is lower than the second level.

10. The device according to claim 8, wherein the read control circuit includes:

a power-on level detecting circuit which detects that the power voltage has reached the second level during a rise to output a power-on reset signal;

a delay circuit which receives the first fuse data and the power-on reset signal and has delay time controlled according to the first fuse data so as to delay the power-on reset signal.

11. The device according to claim 8, wherein the

first fuse data stored in the fuse circuit is chip address data.

12. The device according to claim 10, wherein the delay circuit includes:

a clock signal generating circuit which receives the power-on reset signal so that operation of the generating circuit is controlled according to the power-on reset signal to output a clock signal;

a counter circuit which receives and counts the clock signal; and

a decoder circuit which receives a count output from the counter circuit and the first fuse data so that an output from the decoder circuit is changed after the counter circuit has counted a predetermined number of clock signals, the predetermined number being controlled according to the first fuse data.

13. The device according to claim 10, wherein the delay circuit has at least a resistance circuit and a capacitor circuit, and the delay time is controlled by varying one or both of a resistance value of the resistance circuit and a capacitance of the capacitor circuit according to the first fuse data signal.

14. The device according to claim 8, wherein the fuse circuit includes a laser fuse element.

15. The device according to claim 8, wherein the fuse circuit includes an electric fuse element.

16. A non-volatile semiconductor storage device

comprising:

a ROM region which stores fuse data;

a pulse generating circuit which generates a pulse signal on the basis of a first signal supplied to a first pad;

a delay circuit which receives and delays the pulse signal and has delay time controlled on the basis of a second signal supplied to at least one second pad; and

a ROM read control circuit connected to the ROM region and the delay circuit to control reading of the fuse data from the ROM region according to an output from the delay circuit.

17. The device according to claim 16, wherein the at least one second pad comprises two pads.

18. The device according to claim 16, wherein the delay circuit includes:

a clock signal generating circuit in which operation of the generating circuit is controlled according to the pulse signal and which outputs a clock signal;

a counter circuit which receives and counts the clock signal; and

a decoder circuit which receives a count output from the counter circuit and the second signal so that an output from the decoder circuit is changed after the counter circuit has counted a predetermined number of

clock signals, the predetermined number being controlled according to the second signal.

19. The device according to claim 16, wherein the delay circuit has at least a resistance circuit and a capacitor circuit, and the delay time is controlled by varying one or both of a resistance value of the resistance circuit and a capacitance of the capacitor circuit according to the second signal.

20. A non-volatile semiconductor storage device comprising:

a first non-volatile memory chip having a ROM region which stores fuse data, the first non-volatile memory receiving a power voltage and controlling reading of the fuse data from the ROM region after the power voltage has reached a predetermined level during a rise; and

at least two second non-volatile memory chips having a ROM region which stores fuse data, the at least two second non-volatile memories each receiving the power voltage and controlling reading of the fuse data from the ROM region after the power voltage has reached a predetermined level during a rise, the at least two second non-volatile memory chips having timings for activating an operation of reading the fuse data which timings are different from that for the first non-volatile memory chip and from each other.

21. A non-volatile semiconductor storage device comprising:

a first non-volatile memory chip; and

at least one second non-volatile memory chip, the first non-volatile memory chip includes:

a first ROM region which stores fuse data;

a first pulse generating circuit which generates a first pulse signal on the basis of a first signal;

a first delay circuit which receives and delays the first pulse signal and has delay time for the first pulse signal controlled on the basis of a second signal supplied to at least one second pad; and

a first ROM read control circuit which receives an output from the first delay circuit to control reading of the fuse data from the first ROM region according the output from the first delay circuit;

the at least one second non-volatile memory chip includes:

a second ROM region which stores fuse data;

a second pulse generating circuit which generates a second pulse signal on the basis of the first signal;

a second delay circuit which receives and delays the second pulse signal and has delay time for the second pulse signal controlled on the basis of a third signal supplied to at least one third pad; and

a second ROM read control circuit which receives an output from the second delay circuit to control

reading of the fuse data from the second ROM region according the output from the second delay circuit.